CLAIMS

Having thus described the invention in detail, what we claim as new and desire to secure by Letters Patent is:

1. A semiconducting device comprising:

a channel region located in an SOI layer of an SOI substrate, wherein said channel region is thinned by the presence of an underlying localized oxide region that is located on top of and in contact with a buried insulating layer of said SOI substrate, said localized oxide region is self-aligned to a gate region that is located above said channel region.

2. The semiconducting device of Claim 1 wherein said channel region has a thickness of less than approximately 50.0 nm.

3. The semiconducting device of Claim 1 wherein said channel region has a thickness ranging from approximately 2.0 nm to approximately 25.0 nm.

4. The semiconducting device of Claim 1 further comprising spacers abutting said overlying gate region.

5. The semiconducting device of Claim 1 wherein said SOI layer further comprises source/drain extension regions abutting said channel region.

6. The semiconductor device of Claim 1 wherein said SOI layer comprises Si, SiGe, SiGeC, SiC or combinations thereof.

7. The semiconducting device of Claim 1 wherein said localized oxide region has a thickness ranging from about 25.0 nm to about 65.0 nm.

8. The semiconductor device of Claim 1, wherein said buried insulating layer has a uniform thickness ranging from about 150.0 nm to about 200.0 nm.

9. The semiconductor device of Claim 1 wherein said localized oxide region comprises a thermal oxide, an implanted oxide, or a combination thereof.

10. The semiconductor device of Claim 5 wherein said source/drain extension regions have a thickness ranging from about 30.0 nm to about 70.0 nm.

11. The semiconducting device of Claim 5 wherein source/drain extension regions comprise a doped region of said SOI layer, wherein said dopant is an n-type dopant or p-type dopant.

12. The semiconducting device of Claim 5 further comprising silicide regions positioned on said source/drain extension regions.

13. The semiconducting device of Claim 1 wherein said SOI layer further comprises isolation regions.

14. The semiconductor device of Claim 1 having an external resistance ranging from about 200.0 Ohm/µm to about 400.0 Ohm/µm.

15. A semiconducting device comprising:

a silicon-on-insulator structure comprising an SOI layer located atop a buried insulating layer, said SOI layer having a channel region which is thinned by the presence of an underlying localized oxide region that is located on top of and in contact with said buried insulating layer; and

a gate region located atop said SOI layer, wherein said localized oxide region is self-aligned with the gate region.

16. A method of forming a thin channel MOSFET comprising:

providing an SOI substrate having a buried insulating layer underlying an SOI layer;

forming a pad stack atop said SOI layer;

forming a dummy gate region atop said pad stack;

providing a localized oxide region that is located on top of and in contact with said buried insulating layer thereby thinning a portion of said SOI layer, said thinned portion of said SOI layer defining a channel;

forming source/drain extension regions in said SOI layer abutting said thinned portion of said SOI layer; and

replacing said dummy gate region with a gate region, wherein said localized oxide region is self-aligned with said gate region.

17. The method of Claim 16 wherein said pad stack comprises a pad oxide layer.

18. The method of Claim 16 wherein said providing localized oxide region comprises:

implanting oxygen at least through said dummy gate region to create a dopant profile in a portion of said SOI layer self-aligned to said dummy gate region; and

annealing said substrate to convert said dopant profile into the localized oxide region, said localized oxide region is located on top of and in contact with said buried insulating layer thereby thinning said SOI layer.

19. The method of Claim 18 wherein said dummy gate region comprises a cap atop a sacrificial gate material, said dummy gate region further comprising nitride spacers abutting said dummy gate region.

20. The method of Claim 19 wherein said sacrificial gate material is poly-silicon.

21. The method of Claim 18 wherein said dummy gate region has a height ranging from about 130.0 nm to about 250.0 nm.

22. The method of Claim 18 wherein said implanting oxygen comprises a dopant concentration ranging from $8x10^{16}$ cm^{-2} to $3x10^{17}$ cm^{-2}.

23. The method of Claim 18 wherein said implanting oxygen comprises an implant energy ranging from 30.0 keV to 60.0 keV.

24. The method of Claim 18 wherein said implanting oxygen comprises an ion implantation apparatus having a current beam density ranging form about 5.0 mA cm^{-2} to about 10.0 mA cm^{-2}.

25. The method of Claim 16 wherein said replacing said dummy gate region with said gate region comprises:

forming a blanket oxide layer atop said substrate co-planar with said dummy gate region;

etching said dummy gate region to expose said pad stack;

etching said pad stack selective to said channel region;

forming a gate dielectric layer atop said channel region; and

forming a gate conductor material atop said gate dielectric layer.

26. The method of Claim 25 wherein said replacing said dummy gate with said gate region further comprises forming a conformal nitride liner atop said dummy gate region prior to said forming said blanket oxide layer.

27. The method of Claim 25 wherein said removing said dummy gate region further comprises etching said cap selective to said sacrificial gate material and etching said sacrificial gate material selective to said pad stack.

28. The method of Claim 27 where said sacrificial gate material is removed using chemical deposition etching or KOH stopping atop said pad oxide layer.

29. The method of Claim 25 where said etching said pad stack comprises a chemical oxide removal process including a vapor or plasma of HF and NH_3.

30. The method of Claim 25 where said gate dielectric layer is formed by thermal oxidation.

31. The method of Claim 25 wherein said forming said gate region comprises blanket depositing a gate conductor material atop said blanket oxide layer and atop said gate dielectric and planarizing said gate conductor material until said gate conductor material is coplanar with said blanket oxide layer.